DP-680

USER MANUAL

DUALi Inc.

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We have our development center in South Korea to provide technical support. For any technical assistance can contact our technical support team as below;

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Revision History

- 2017.06 (Ver. 1.00): First Release

- 2018.04 (Ver. 1.10): Add Memory structure and security method

- 2018.08(Ver. 1.20): Add Instrument size and weight

- 2019.03(Ver. 1.30): Add connector and pin specification

- 2020.04 (Ver. 1.31) : Add drawing of back- plate

Contents

1 Introduction

DP-680 is designed as multi type Contactless payment acceptance device. It is suitable for unattended machine, Kiosk, ATM as well as NFC acceptance dongle for Retails.

This device features serial RS-232 and USB 2.0 communications to POS systems.

The following features are supported:

- ISO14443 type A/B and Mifare based contactless payment transactions
- ISO 18092
- FeliCa
- Mifare, Mifare Desfire EV1, EV2
- ISO 15693
- ISO 7816: 6 x SAM card slots

1.1 Basic specification

ITEM	Specification	Note
CPU	STM32F405RGT6 (ARM Cortex_M4)	
Program Memory	1MBytes FLASH	
Data Memory	192KBytes SRAM	
DISPLAY	4 Status LED (GREEN)	
Communication	USB (Default/ 10 Ω, 3m USB cable without ferrite core) RS-232/ TTL Option	Baud: 115200
BUZZER	Magnetic Buzzer	
Contactless	ISO-14443 A/B, Mifare, DESFire, FeliCa, ISO-15693 NFC	
Contact SAM	ISO-7816: 6 SAM SLOTS	
Input power	DC 5V	

1.2   **RF PART Specification**

ITEM	Speciation	Note
Frequency	13.56MHz	PN5180
Communication speed	106,212,424,848 Kbps	
subcarrier	847 KHz	
Operating voltage	5V	

1.3   **SAM PART Specification**

ITEM	Speciation	Note
Protocol	T=0, T=1	
Class	Class A, B (5V, 3V)	
Quantity	6	

2 Components Confirmation

2.1 Product Components

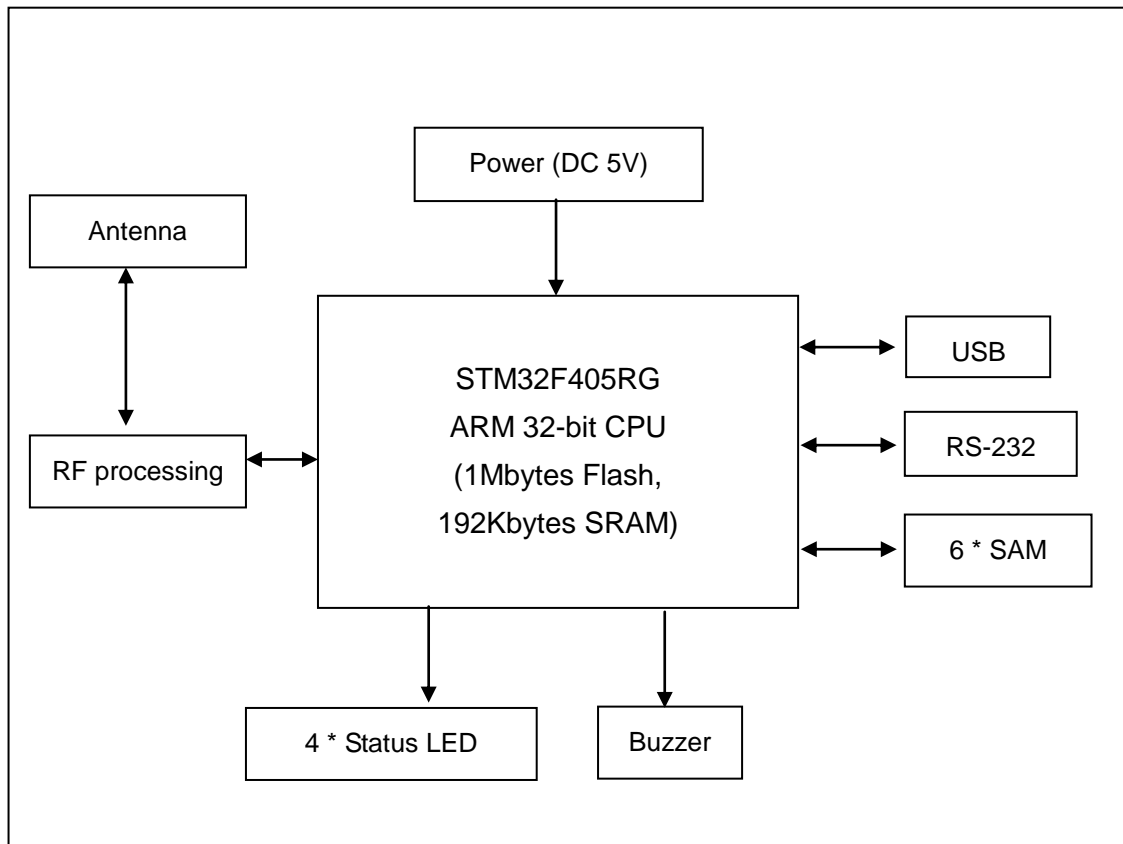① Reader unit: USB cable (default) or Serial cable

DP-680 w/ Option Vessel

DP-680 w/ Standing leg

2.2 Block Diagram

```
                    ┌──────────────────────┐
                    │    Power (DC 5V)     │
                    └──────────┬───────────┘
                               │
  ┌──────────────┐             ▼
  │   Antenna    │   ┌──────────────────────┐      ┌──────────┐
  └──────┬───────┘   │                      │◄────►│   USB    │
         ▲           │    STM32F405RG       │      └──────────┘
         │           │    ARM 32-bit CPU    │
         ▼           │    (1Mbytes Flash,   │◄────►┌──────────┐
  ┌──────────────┐   │    192Kbytes SRAM)   │      │  RS-232  │
  │RF processing │◄─►│                      │      └──────────┘
  └──────────────┘   │                      │◄────►┌──────────┐
                     └─────┬──────────┬─────┘      │  6 * SAM │
                           │          │            └──────────┘
                           ▼          ▼
                  ┌──────────────┐ ┌──────────┐
                  │4 * Status LED│ │  Buzzer  │
                  └──────────────┘ └──────────┘
```

- MAIN MCU: ARM CORTEX 32-bit M4 RISC processor
- RF Processing: PN5180 to support ISO14443A/B, ISO15693, Mifare series, DESFires EV1 & EV2, FELICA
- Host Communication: USB or RS-232
- Buzzer: Frequency controllable buzzer.
- Status LED: EMV compliant LED * 4ea.
- Power: Input power DC5V.
- SAM Communication: Max. 6pcs SAM support. Up to 153600bps.
  Clock controllable up to 18MHz by FDK

2.3 Exterior

< Front >   < Rear >

- Dimension (mm)
  - 110.2(W) * 80.1(D) * 20.0(L)

Screw hole for bracket (4ea)

<Insert screw hole drawing>
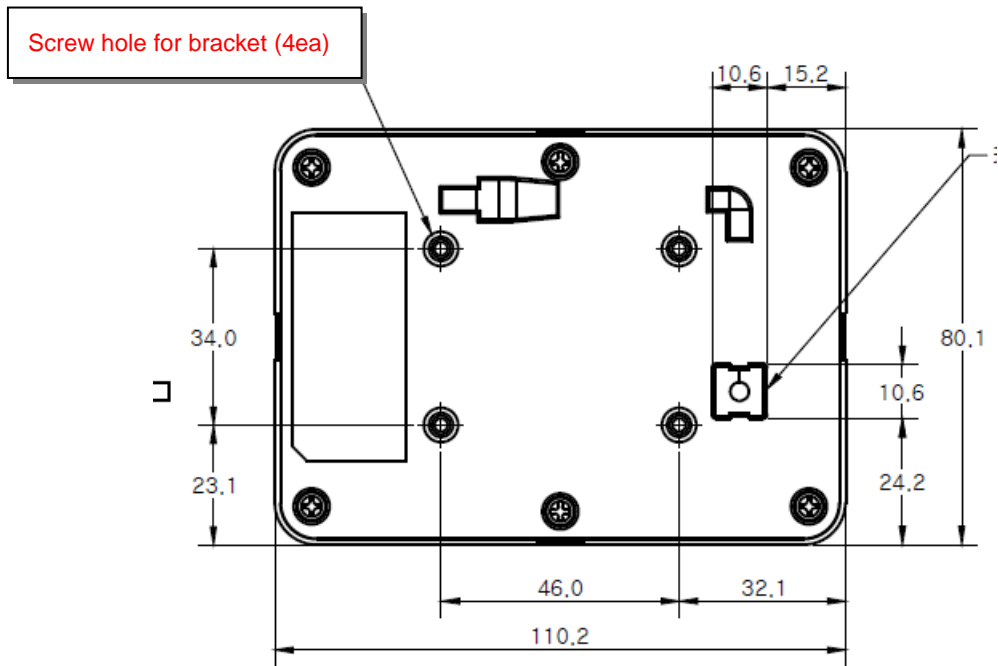
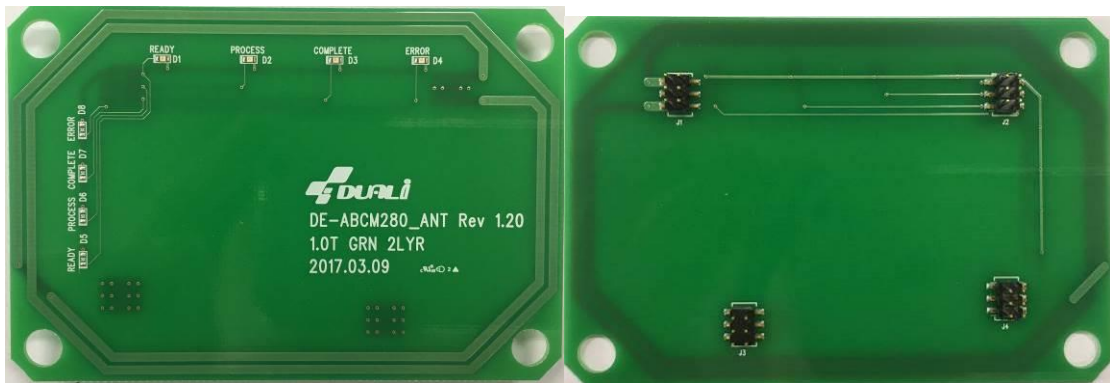### 2.4 PCB
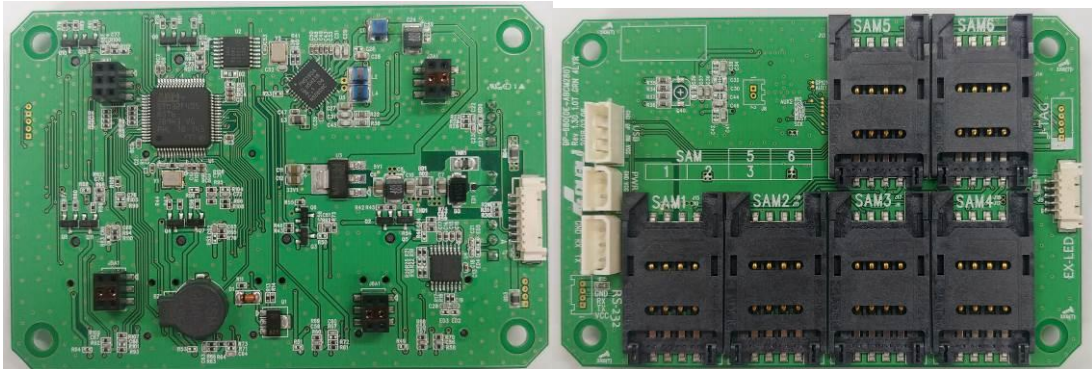
- MAIN Board

- Main Board Top -

- Main Board Bottom -

- Antenna Board Top -

- Antenna Board Bottom -

2.5 Flash Memory Structure

Sector	Address	Size	Usage
Sector 0	0x0800 0000 - 0x0800 3FFF	16 Kbytes	BIOS
Sector 1	0x0800 4000 - 0x0800 7FFF	16 Kbytes	
Sector 2	0x0800 8000 - 0x0800 BFFF	16 Kbytes	**PARAMETER and Key**
Sector 3	0x0800 C000 - 0x0800 FFFF	16 Kbytes	RFU
Sector 4	0x0801 0000 - 0x0801 FFFF	64 Kbytes	Application
Sector 5	0x0802 0000 - 0x0803 FFFF	128 Kbytes	
Sector 6	0x0804 0000 - 0x0805 FFFF	128 Kbytes	
Sector 7	0x0806 0000 - 0x0807 FFFF	128 Kbytes	
Sector 8	0x0808 0000 - 0x0809 FFFF	128 Kbytes	
Sector 9	0x080A 0000 - 0x080B FFFF	128 Kbytes	RFU
Sector 10	0x080C 0000 - 0x080D FFFF	128 Kbytes	RFU
Sector 11	0x080E 0000 - 0x080F FFFF	128 Kbytes	Fare Table

2.6 Flash Protection

1.6.3 Read protection (RDP)

The user area in the Flash memory can be protected against read operations by an entrusted code. Three read protection levels are defined:

- Level 0: no read protection

  When the read protection level is set to Level 0 by writing 0xAA into the read protection option byte (RDP), all read/write operations (if no write protection is set) from/to the Flash memory or the backup SRAM are possible in all boot configurations (Flash user boot, debug or boot from RAM).

- Level 1: memory read protection.

  It is the default read protection level after option byte erase. The read protection Level 1 is activated by writing any value (except for 0xAA and 0xCC used to set Level 0 and Level 2, respectively) into the RDP option byte. When the read protection Level 1 is set:

  – No Flash memory access (read, erase, program) is performed while the debug features are connected or boot is executed from RAM. A bus error is generated in case of a Flash memory read request. Otherwise all operations are possible when Flash user boot is used or when operating in System memory boot mode.

  – When Level 1 is active, programming the protection option byte (RDP) to Level 0 causes the Flash memory and the backup SRAM to be mass-erased. As a result the user code area is cleared before the read protection is removed. The mass erase only erases the user code area. The other option bytes including write protections remain unchanged from before the mass-erase operation. The OTP area is not affected by mass erase and remains unchanged.

    Mass erase is performed only when Level 1 is active and Level 0 requested. When the protection level is increased (0->1, 1->2, 0->2) there is no mass erase.

- Level 2: Disable debug/chip read protection

  When the read protection Level 2 is activated by writing 0xCC to the RDP option byte, all protections provided by Level 1 are active, system memory and all debug features (CPU JTAG and single-wire) are disabled when booting from SRAM or from system memory, and user options can no longer be changed.

  Memory read protection Level 2 is an irreversible operation. When Level 2 is activated, the level of protection cannot be decreased to Level 0 or Level 1.

Note: *The JTAG port is permanently disabled when Level 2 is active (acting as a JTAG fuse). As a consequence, boundary scan cannot be performed. STMicroelectronics is not able to perform analysis on defective parts on which the Level 2 protection has been set.*

2.7　Key Saving Method

- － Save Key in **PARAMETER and Key** area.
- － All Flash area is protected against read (level1, Reading flash memory with JTAG debugger is impossible).
- － User Key data is accessible only with firmware function.
- － Write User Key function save key after encryption.
- － Read User Key function returns key after decryption.
- － User Key en/decryption Key is different for each reader. (drive key from unique ID number of MCU)

3　Power & Interface Specification

3.1　Power Specification

- － DC 5V

3.2　Electric Current consumption

- － 5V : average 220mA
- － 5V : Max 400mA (Card detecting, Card writing)

3.3　RS-232 Interface Specification

- － 115200bps (TTL Option)

3.4　USB Interface Specification

- － USB 1.1 Full Speed(12Mbps)

4　Usage Environment

4.1　Operating Environment

- － Temperature: -10 ~ 60　℃
- － Humidity: 30 ~ 90 % (Relative humidity)

4.2　Storage Environment

- － Temperature: -20 ~ 80　℃
- － Humidity: 30 ~ 90 % (Relative humidity)

5 Connector & PIN Specification

5.1   J3 – 1.25mm 4pin (DEBUG) – optional connector

PIN	Specification	NOTE
1	PWR_IN_5V	
2	TXD	RS-232
3	RXD	RS-232
4	GND	

5.2   J4 – 2.5mm 3pin(RS-232) / YMW025-03R (Wafer), YMH025-03R (Housing)

PIN	Specification	NOTE
1	TXD	RS-232
2	RXD	RS-232
3	GND	

5.3   J5 – 1.25mm 5pin (LED) / 12505WR-05 (Wafer), 12505HS-05 (Housing)

PIN	Specification	NOTE
1	LED_READY	
2	LED_PROCESS	
3	LED_COMPLETE	
4	LED_ERROR	
5	VDD 5.0V	

5.4   J6 – 2.0mm 4pin (USB) / 20017WS-04A (Wafer), 20017HS-04 (Housing)

PIN	Specification	NOTE
1	PWR_IN_5V	
2	USB_DM	
3	USB_DP	
4	GND	

5.5   J7 – 1.25mm 7pin (USB & RS232) / 12505WR-07 (Wafer), 12505HS-07 (Housing)

PIN	Specification	NOTE
1	PWR_IN_5V	
2	USB_DM	
3	USB_DP	
4	TXD	RS-232
5	RXD	RS-232
6	GND	
7	GND	

6 Weight

- 210g (Include cable)

7 Warning and Notice

- Indoor use only (Avoid direct sunlight)

- Avoid an element like metal or magnetism within 7cm

- Do not open the product or adjust the antenna part

8 Warranty & Service

‣ Warranty and Repair service

- DUALi Inc. warrants to the original consumer or other end user that this product, DP-680, is free from defects in materials and workmanship for a period of 1 year from the date of purchase.

※ **Note** Warranty/non-warranty repair fees do not include any shipping charges.

‣ The damages(defaults) prescribed below are NOT to be covered by warranty.

- User's misuse of part/component.
- Fault by the unqualified user's own intention of repairs.
- Product's inspection requirement.
- Adding certain functions or extension of system.
- Fault by User's misuse against the product's manual.

*Please contact our service team for the technical/ sales supports.

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