Higgs™ 4 IC Datasheet

An

EPCglobal Compliant

Class-1 Generation-2

And

ISO/IEC 18000-6C

UHF RFID Integrated Circuit

Draft – V1.3.7

October 2016

Contents

LIST OF FIGURE

Revision History

Revision	Date	Description of Major Changes	Author of Changes
1.0.0	May 15, 2012	Initial release	Neil Mitchell
1.1.0	July 24, 2012	Order information updated (a) include updated IC ordering information and (b) added Strap	Neil Mitchell
1.2.0	Sept 6th 2012	Added Strap information	Neil Mitchell
1.3.0	Dec 4, 2012	Added Reel information for the Strap; added SOT; added wafer/die orientation (1.3.1 & 1.3.2) – March 2013 Updated Storage temp (V1.3.3) – July 2013 Added wafer frame dims (V1.3.4) – May 2014 Added directivity (V1.3.5) - June 2014	Neil Mitchell
1.3.6	July 25, 2016	Removed verboten reference	Tom Trexler

1 Introduction

Table 1.1 - Higgs4 IC Major Features

FEATURE	DESCRIPTION	BENEFIT
Further Increases Alien's Industry Leading Read Sensitivity	Industry leading tag performance especially in challenging RF environments.	Saves money: Reduces the number of read points and/or minimizes tag size.
Enhanced Write Sensitivity	Cutting edge write sensitivity.	Increased write performance, writing multiple words in a single command and writing to multiple-tags simultaneously, massively decreases the cost and time associated with programming millions of tags. Blastwrite is proven up to 3,600 tags/minute (measured performance).
Quick**Write**™	The ability to write a complete bank of memory with one command.	
Blast**Write**™	An IC mass-encoding capability with compatible Readers. Takes a single write-cycle to encode multiple tags.	
Optimized Memory Footprint for Volume Applications	Flexible memory architecture that provides for the optimum allocation of EPC and User memory.	Provides an optimal memory system for volume applications while addressing the needs of enterprise-wide serialization.

Higgs-4 ICs operate at extremely low power levels yet still provides sufficient backscatter signal to read tags at extended range. It can also be programmed at low RF power and at high speed using Alien's QuickWrite™ single instruction bank-write capability. Alien's BlastWrite™ capability can also be used to program multiple tags simultaneously for mass-encoding in high-volume retail applications. Higgs-4 ICs also fully support the latest industry standard serialization schemes.

Higgs-4 ICs offer a mass-market optimized but flexible memory architecture that provides for the optimum allocation of EPC and User memory for different use cases such as legacy part numbering systems and service history. User memory can also be read and or write locked on 32-bit boundaries, supporting a variety of public/private usage models.

Higgs-4 ICs contains a number of unique advanced features. Alien's Dynamic Authentication™ feature provides a unique non-reproducible fingerprint that can be used for anti-cloning and anti-counterfeiting.

The IC also features factory programmed 64-bit serial number that cannot be altered. In conjunction with the EPC code, this provides a unique identification for the tagged item.

This document specifies the operational and parametric requirements for Alien Technology®'s Higgs 4 IC, an EPCglobal Class-1 Generation-2 (V 1.2.0) and ISO/IEC 18000-6C compliant IC.

Higgs 4 IC is a self-contained SoC device that when assembled with an antenna completes a passive RFID tag. The EPCClass-1 Generation-2 specification is referred herein as the "EPCglobal", and defines and specifies operation of Interrogator-Tag systems.

Applications for Higgs 4 IC include:

- supply chain management (SCM)
- distribution logistics
- asset inventory and tracking
- airline baggage handling and identification
- express parcel ID, tracking and delivery
- item level tagging
- remote article identification
- factory automation

- brand protection
- object theft detection

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2 Identification

This application note applies to Higgs 4 IC's manufactured by Alien Technology which has the manufacturing code specified below in the TID. These values may be read using the protocol Read command at the word offsets indicated. The features described in this application note may vary in other IC's.

Table 2.1: Applicable TID Values

Membank	Offset	Contents	Meaning
TID	0	0xE200	EPCglobal ACI, Alien Manufacturer Code upper bits
TID	1	0x3414	Alien Manufacturer Code lower bits, Higgs 4 IC

3 Higgs 4 IC Overview and Architecture

3.1 Overview

3.1.1 Device Power

The Higgs 4 IC is connected via two terminals to a suitable antenna, together comprising a Tag. Higgs 4 IC operating power is derived from RF energy transmitted by an Interrogator and coupled through the Tag Antenna into the Device.

3.1.2 Interrogator-to-IC Communication

Interrogators modulate their RF transmission in order to communicate commands and information to the IC. The Interrogator sends binary information to the IC by modulating the phase and/or amplitude of its RF transmission using pulse interval encoding. Modulated Interrogator transmissions appear as amplitude modulated RF envelope at the IC terminals, independent of the modulation type allowed by EPCglobal (DSB-ASK, SSB-ASK, or PR-ASK). After issuing a command, the Interrogator transmits unmodulated RF energy to maintain IC operating power while it awaits a reply from the IC.

3.1.3 IC-to-Interrogator Communication

The IC follows an “Interrogator talks first” (ITF) protocol, and will not execute a command unless it is valid and appropriate for the IC. The IC will not respond until the Interrogator has completed its command transmission. The IC replies to Interrogator commands by modulating its input impedance, causing modulation of the RF amplitude and phase reflected by the Tag antenna. Interrogators detect the variation in reflected RF, demodulate and decode the Tag reply. An Interrogator may transmit a series of commands in order to access data stored in the IC, to set operating states, or to write information into the tags NVM memory.

3.1.4 Memory

The IC contains a total of 544 bits of memory, of which 320 bits are customer programmable and 448 bits are NVRAM/RAM. These 320 bits include 128 bits of NVM for Electronic Product Code (EPC) data, 128 bits of NVM for User data and 64 bits of NVM for Reserve data (Passwords). Alien-specific data is also stored in the NVM which is not customer programmable. Individual NVM bits may be programmed to the logical “0” or “1” states through programming commands. NVM memory may be locked to prevent tampering or inadvertent data corruption. The IC may be killed to prevent subsequent use. A completed kill sequence results in a permanently deactivated tag.

4 Specifications

4.1 Absolute Maximum Ratings

Table 4.1 – Absolute maximum ratings

Parameter Name	Units	Maximum Rating	Conditions	Comments
ESD Withstand Capability (HBM)	V_{peak}	2000	+25 °C	Survive 3 positive and 3 negative events at the rated voltage with no performance degradation.

Table 4.2 – Environmental and physical specifications

Parameter	Symbol	Units	Min	Typ	Max	Conditions	Comments
Storage Temperature	T_{STOR}	°C	-50		85		
Nominal operating temperature	T_{NOM}	°C	-50	25	85		
Relative humidity		%			98	Packaged in tag	Non-condensing
Die size, per side		µm	-	589.5	-	Center to center die pitch on wafer	

4.2 Key Electrical Specifications

Unless otherwise noted, parameters are specified over the temperature range of -30 °C to +70 °C; command input data rate corresponding to a TARI=6.25µs-25µs; data "1" width = 1.5Tari; reply LF = 250 kHz in Miller 4 backscatter modulation mode.

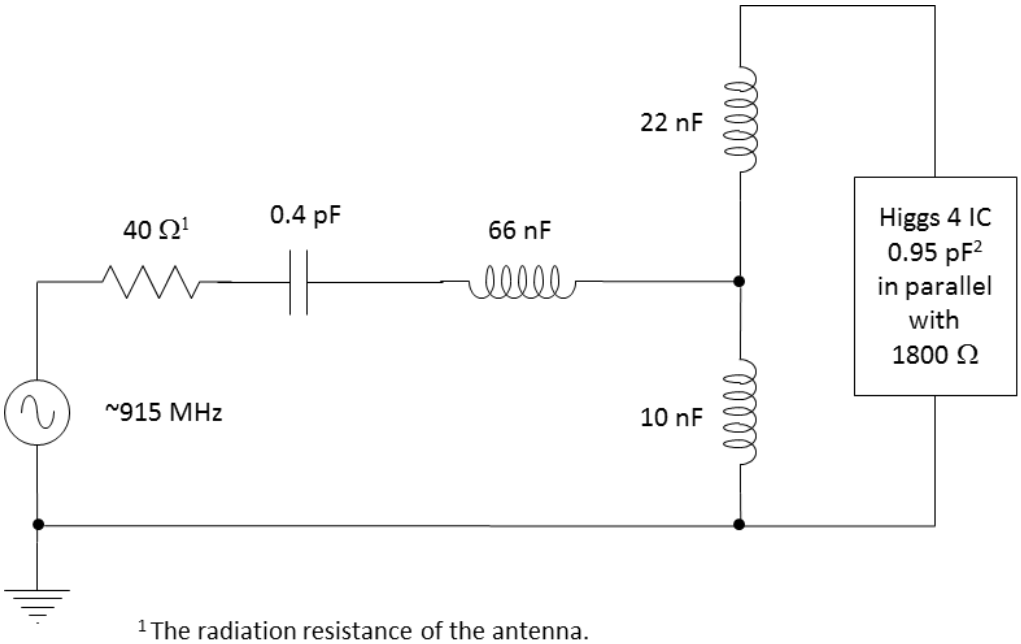
Table 4.3 – Key electrical specifications

Parameter	Symbol	Units	Min.	Typ.	Max.	Conditions	Comments
RF Frequency	RF	MHz	860	915	960		
RF parallel equivalent input capacitance	C_{in}	pF		0.85 (chip alone) 0.95 (SOT/Tag) 0.89 (strap)		25 °C	@ minimum operational power
RF parallel equivalent input resistance	R_{in}	Ω		1800			
Minimum RF communication power	P_{com}(min)	dBm		-20.5		TARI=25µs, 25 °C	With 2dBm directivity of dipole
Minimum RF programming power	P_P(min)	dBm		-17		25 °C, @ matched parameters as specified for example in Fig 5.1	Word write (16-bits). With 2dBm directivity of dipole
NVM Use model		cycles	100,000			At 25°C	
NVM data retention		years	50				

5 Reference antenna design

Figure 2 is an example of a broadband tag such as an Alien Squiggle™. The lumped elements shown in the figure are a representative model of a possible antenna design.

Figure 1 – Reference equivalent circuit of a broadband antenna such as the Alien Squiggle™.



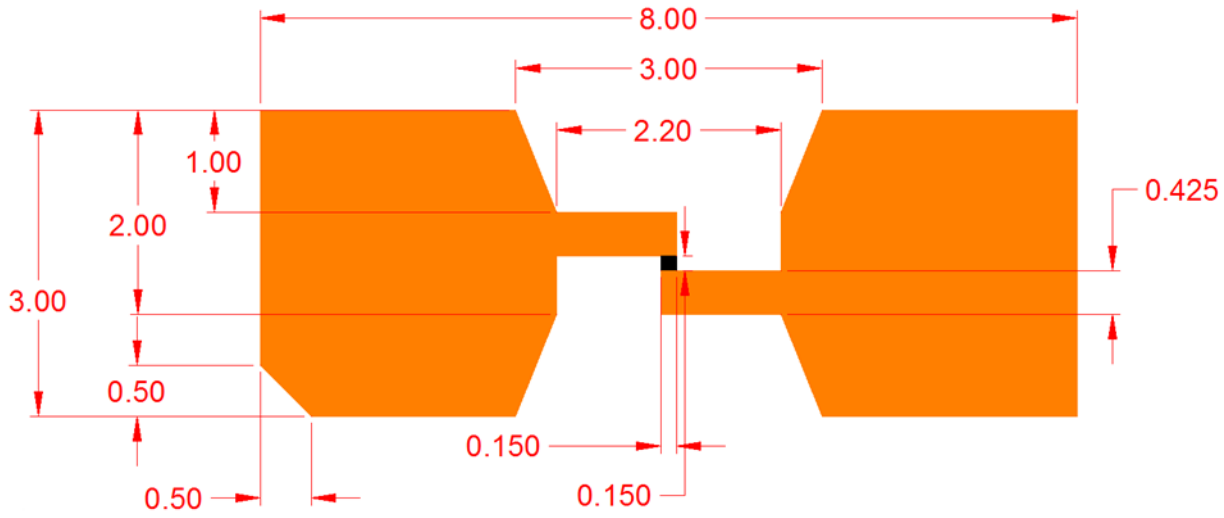
[1] The radiation resistance of the antenna.

[2] (a) The **flip chip** assembly adds 0.05 to 0.15 pF to the capacitance of the IC (e.g. 0.85pF + 0.1pF shown)
(b) The **strap** assembly adds 0.04 pF (in parallel) to the capacitance of the IC (not included above)

6 Strap Simulation

The following information allows modelling of the Higgs4 strap.

Figure 2 - Strap Dimensions for Simulation



For the purpose of simulation, the following application characteristics should be used:

Figure 3 - Higgs4 Strap Application Model

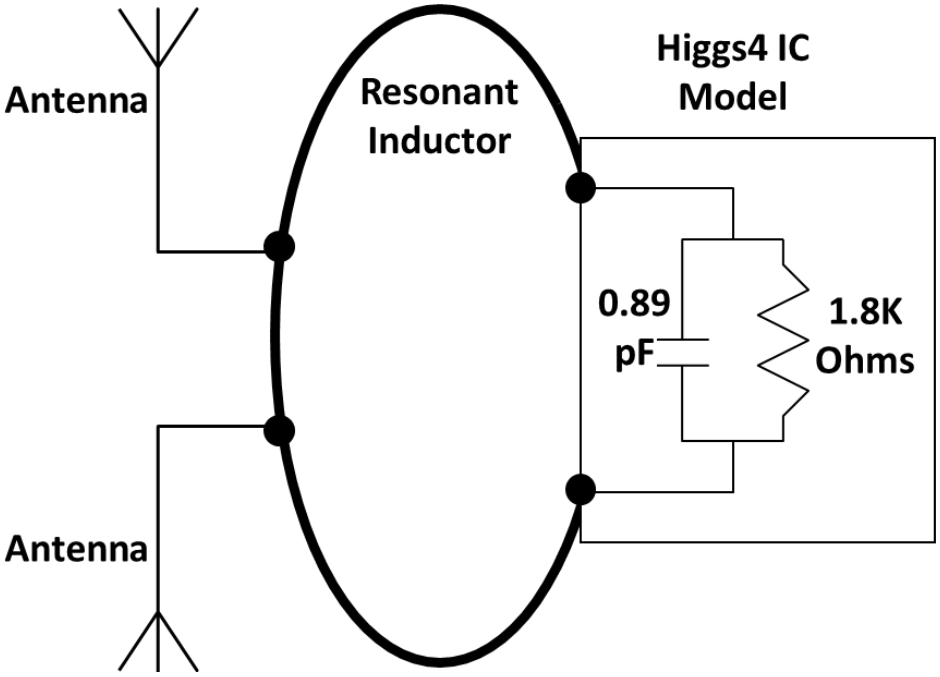
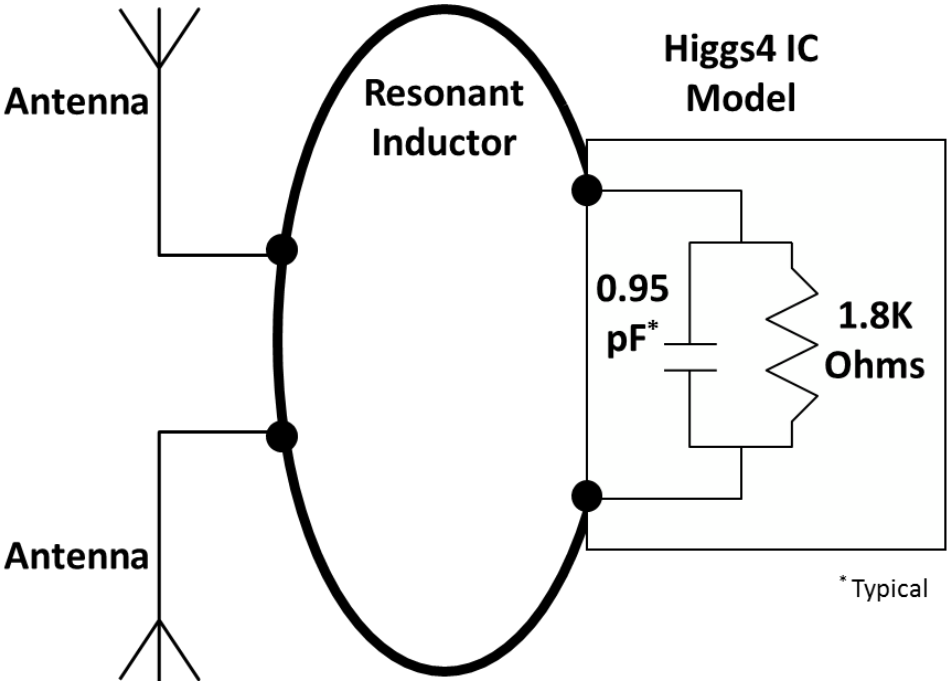


Figure 4 - Higgs4 SOT Application Model



7 Memory

7.1 Memory Map

The following shows a high-level view of the Higgs-4 memory map.

Table 7.1 - High-Level Higgs4 Memory Map

Bank	Address	Description	Memory	Bits
User	00h – 7Fh	User	NVM	128
TID	60h – BFh	Device Configuration	ROM-NVM	96
	20h – 5Fh	Unique Tag ID Unalterable	NVM	64
	00h – 1Fh	TID EPC/TMD/TMDID/TMN	ROM	32
EPC	20h – 9Fh	EPC #	NVM	128
	10h – 1Fh	EPC-PC	NVM	16
	00h – 0Fh	EPC-CRC	RAM	16
Reserved	20h – 3Fh	RES-Access Pwd, EPC optional	NVM	32
	00h – 1Fh	RES-Kill Pwd	NVM	32

The following table is the memory map as seen by commands which use bank and offset pointers (logical addressing):

Table 7.2 - Detailed Logical Memory Map

Reserved (System) Bank Bit transmission order into or out of Device →																
Reserved Bank [00], Row 0	**Kill Password (hi), (NVM)**															
Field Name >	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Reserved Bank [00], Row 1	**Kill Password (lo), (NVM)**															
Field Name >	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW	KPW
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Reserved Bank [00],	**Access Password (hi), (NVM)**															

Row 2																
Field Name >	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	20	21	22	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

Reserved Bank [00], Row 3	**Access Password (lo) (NVM)**															
Field Name >	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW	APW
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F

EPC Bank
Bit transmission order into or out of Device →

EPC Bank [01], Row 0	**EPC CRC (Register, Read Only)** (calculated at power-up & stored at this address)															
Field Name >	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

EPC Bank [01], Row 1	**Protocol Control (NVM)**															
Field Name >	LEN	LEN	LEN	LEN	LEN	UMI (Reg Read Only)	(Reg Read Only)	NSI	NSI	NSI	NSI	NSI	NSI	NSI	NSI	NSI
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Value >							0									

EPC Bank [01], Row 2	**Electronic Product Code (NVM)**									**EPC Word 0 (MS)**						
Field Name >	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address >	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F

EPC Bank [01], Row 3	**Electronic Product Code (NVM)**										**EPC Word 1**					
Field Name >	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F

EPC Bank [01], Row 4	**Electronic Product Code (NVM)**										**EPC Word 2**					
Field Name >	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

EPC Bank [01], Row 5	**Electronic Product Code (NVM)**	**EPC Word 3**

Field Name >	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
EPC Bank [01], Row 6	**Electronic Product Code (NVM)**										**EPC Word 4**					
Field Name >	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F
EPC Bank [01], Row 7	**Electronic Product Code, (NVM)**										**EPC Word 5**					
Field Name >	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
EPC Bank [01], Row 8	**Electronic Product Code, (NVM)**										**EPC Word 6**					
Field Name >	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
EPC Bank [01], Row 9	**Electronic Product Code, (NVM)**										**EPC Word 7**					
Field Name >	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC	EPC
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F

TID Bank
Bit transmission order into or out of Device →

TID Bank [10], Row 0	**EPC / ISO / Manufacturer Codes (hi), (ROM)**															
Field Name >	ACI	ACI	ACI	ACI	ACI	ACI	ACI	ACI	TMDI	TMDI	TMDI	TMDI	TMDI	TMDI	TMDI	TMDI
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Value >	***1***	***1***	***1***	***0***	***0***	***0***	***1***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***
Info >	EPCglobal Allocation Class Indicator								Alien Mfr Code (upper bits)							
TID Bank [10], Row 1	**EPC / ISO / Manufacturer Codes (lo), (ROM)**															
Field Name >	TMD	TMD	TMD	TMD	TMN	TMN	TMN	TMN	TMN	TMN	TMN	TMN	TMN	TMN	TMN	TMN
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Example Value >	***0***	***0***	***1***	***1***	***0***	***1***	***0***	***0***	***0***	***0***	***0***	***1***	***0***	***1***	***0***	***0***
Info >	Alien Mfr Code (Lo bits)				Model Series = 4 (Higgs)				Major Rev. = 1				Minor Rev. = 4			
TID Bank [10], Row 2	**Unique ID Word 0, (NVM) (MS Word)**															

Field Name >	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
Value (UID Mask) >	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***

TID Bank [10], Row 3	**Unique ID Word 1, (NVM)**															
Field Name >	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
Value (UID Mask) >	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***

TID Bank [10], Row 4	**Unique ID Word 2, (NVM)**															
Field Name >	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
Value (UID Mask) >	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***

TID Bank [10], Row 5	**Unique ID Word 3, (NVM) , (LS Word)**															
Field Name >	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID	UID
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
Value (UID Mask) >	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***	***0***

TID Bank [10], Row 6	**Reserved, (ROM)**															
Field Name >																
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F

TID Bank [10], Row 7	**Reserved (ROM and Read Only Register)**															
Field Name >	Reserved				Reserved											
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F

TID Bank [10], Row 8	**Reserved (Read Only register and ROM)**															
Field Name >	Reserved				Reserved											
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F

TID Bank [10], Row 9	**Reserved (NVM)**															
Field Name >	Reserved															
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F

TID Bank [10], Row 10	**Reserved (NVM)**															
Field Name >	Reserved															
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF

TID Bank [10], Row 11	**Reserved (NVM)**															
Field Name >	Reserved															
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF

User Bank
Bit transmission order into or out of Device →

User Bank [11], Row 0	**User ID, (NVM)**								**MS Word**							
Field Name >	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Info>				A logic "1" value in any bit cell signals data in User Bank for calculating XI bit in PC												

User Bank [11], Row 1	**User ID, (NVM)**															
Field Name >	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

User Bank [11], Row 2	**User ID, (NVM)**															
Field Name >	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F

User Bank [11], Row 3	**User ID, (NVM)**															
Field Name >	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F

User Bank [11], Row 4	**User ID, (NVM)**															
Field Name >	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

User Bank [11], Row 5	**User ID, (NVM)**															
Field Name >	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F

User Bank [11], Row 6	**User ID, (NVM)**															
Field Name >	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F

User Bank [11], Row 7	**User ID, (NVM)**

Field Name >	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User	User
Field Bit # >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External Hex Bit Addres	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F

1: The TID bank is only writable using proprietary commands, and is always locked and permalocked

8 Supported Commands

Note that the form of the required and optional commands is specified in the EPCGlobal Gen 2 v 1.2 protocol documentation. All mandatory EPCglobal commands are supported including the following optional and custom commands. For further details on usage of custom commands please reference the “Custom Command Usage Addendum” (available under special legal agreement from Alien Technology).

Optional commands as specified in EPCglobal that are supported are

1. BlockWrite: This enables QuickWrite™ feature as detailed earlier. This can write an entire memory bank in one command. Word pointer can be at any word in the bank and the word count can be to the end of the bank
2. BlockPermaLock: Block lengths are 32 bits and a total of 4 blocks

Custom commands

1. BlockReadLock: Allows the blocks of the user memory to be read locked
2. Status: Allows direct reading of chip lock status
3. Ping: Enables the BlastWrite™ feature

9 Physical Attributes

9.1 Physical Dimensions and Bump Map (Flip Chip)

This shows the location of the flip-chip bumps and which are to be connected and how.

Figure 5 - Top Die View (dimensions in μm)

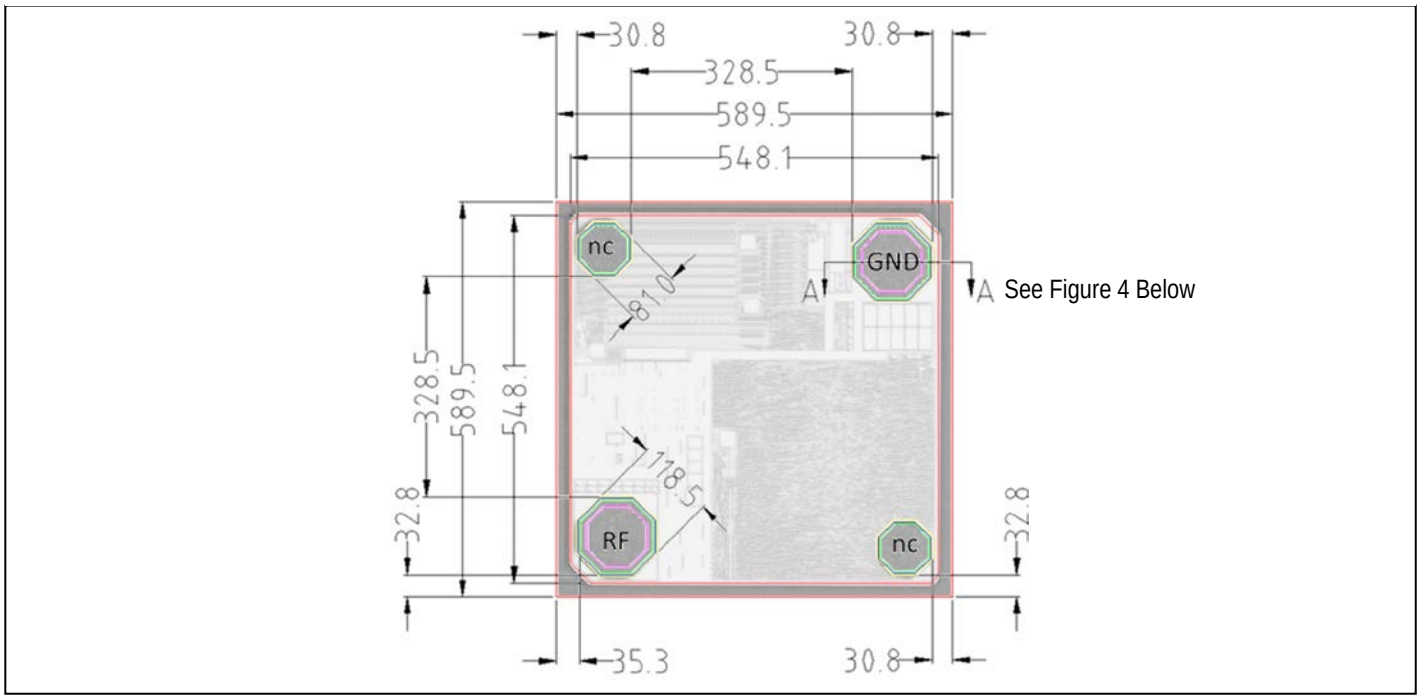


Figure 6 - Cross Section (A) of GND/RF Gold Bump and Wafer (dimensions in μm)

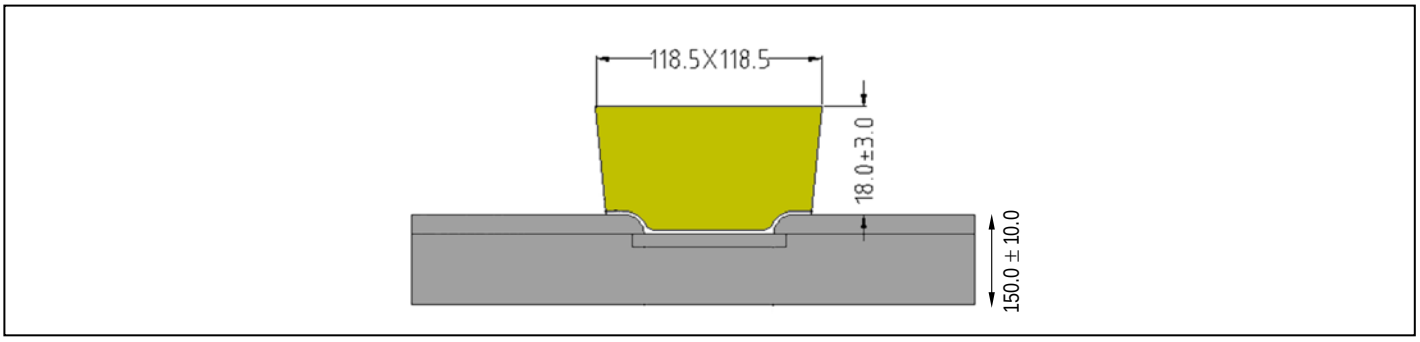
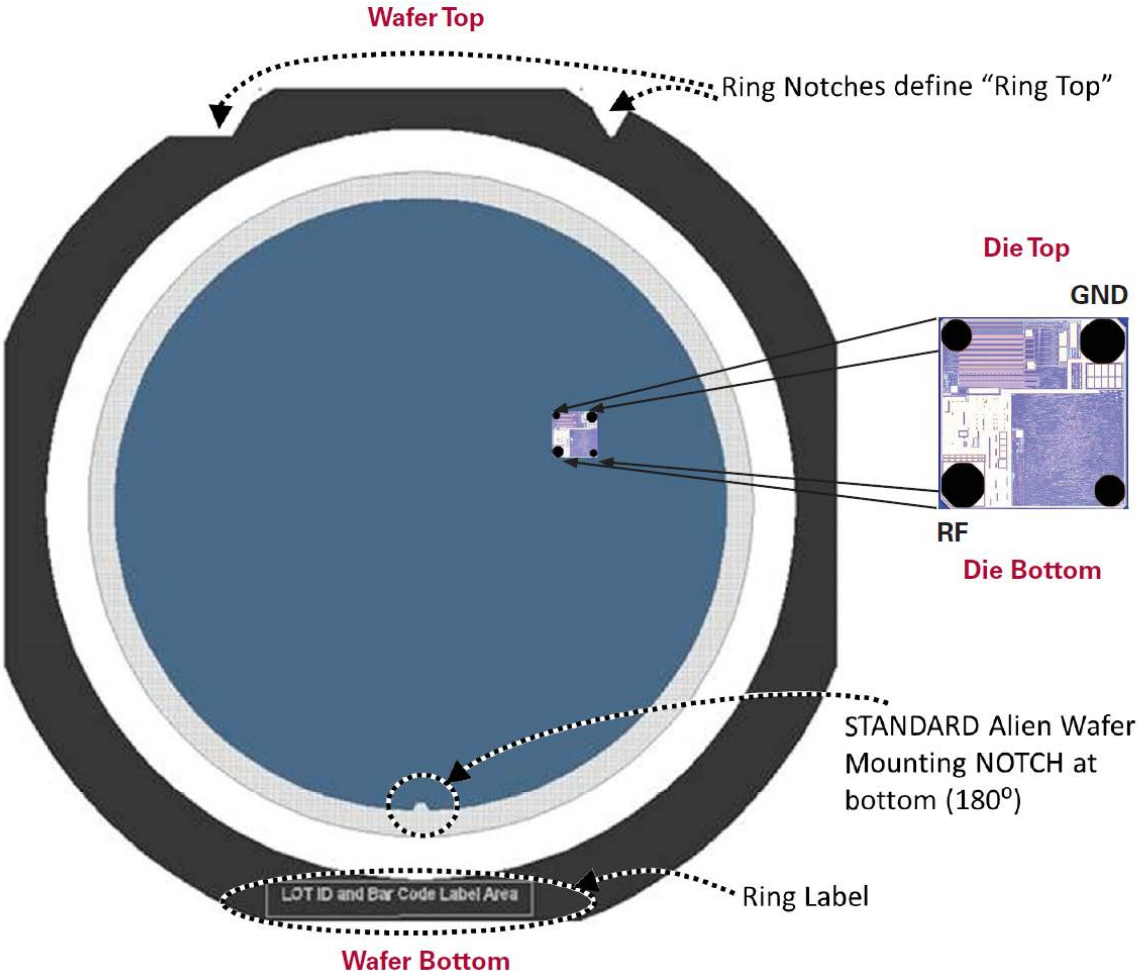


Figure 7 - Wafer / Die orientation



For 200 mm wafer:

10.886" x 10.886" x .045" thick steel (276 mm x 250 mm x 1.22 mm)

Equivalent to:

Disco model DTF2-8-1 p/n MDTFR200-01,

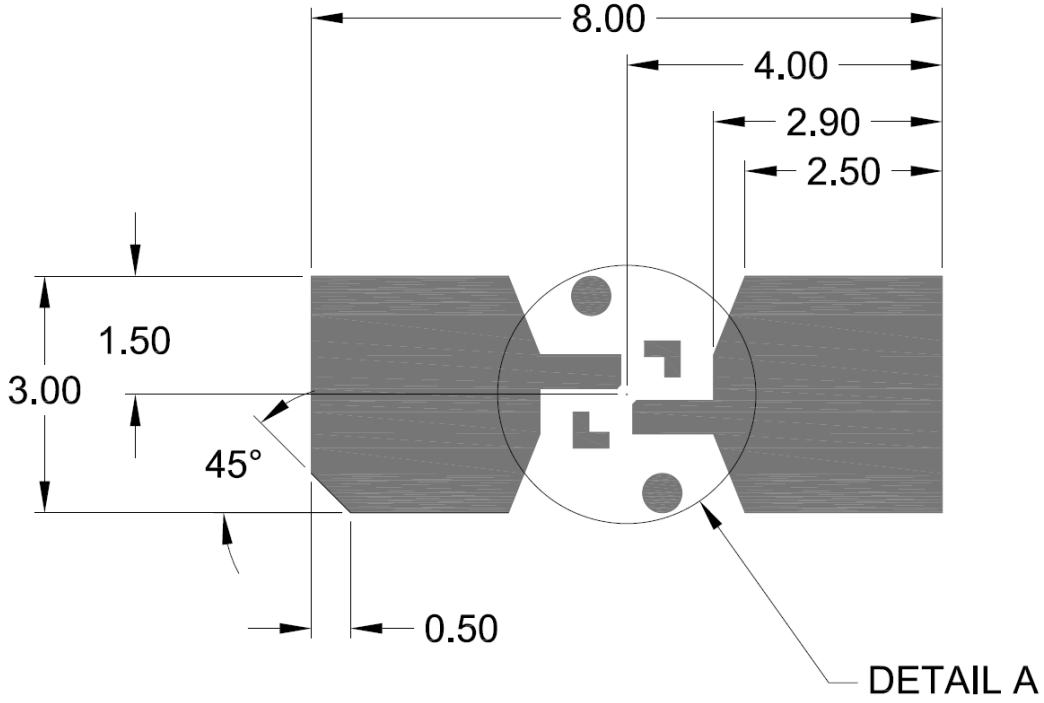
Topline FF-108,

Precision Products FF-108

Epak mOP0311

9.2 Physical Dimensions (Strap)

Figure 8- High Level Strap Dimensions (with alignment marks shown as supplied on strap)



Note:

(1) This shows the alignment marks used by Alien for chip mounting. These are part of the strap as provided.

(2) This diagram does not show the IC mounted in the strap.

Figure 9 - Detail A For Above Diagram

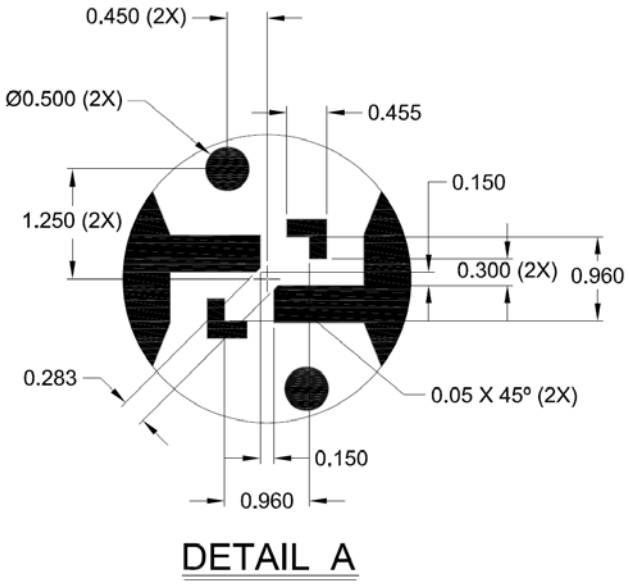


Figure 10 - Higgs4 Strap Tape Dimensions (JEDEC MO-283 Variant AA)

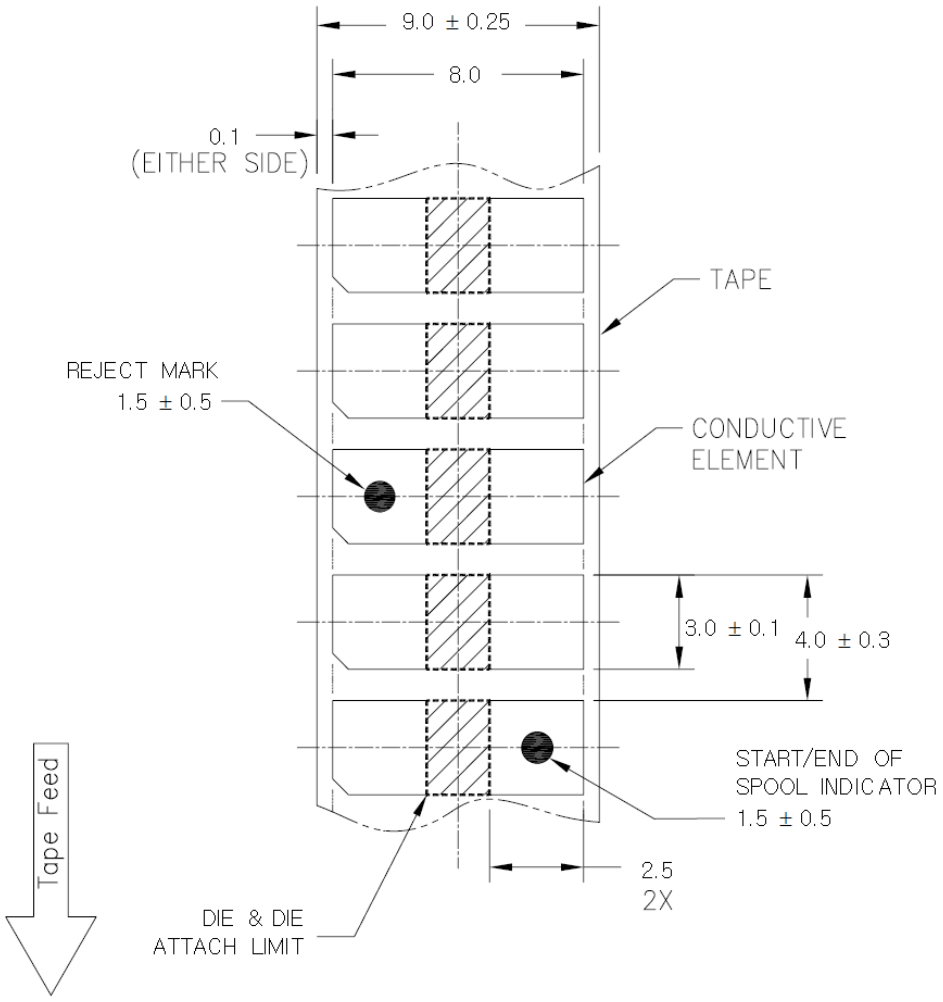


Table 9.1- Strap Reel Parameters

Parameter	Rating
Outside Diameter	13" [33cm]
Inside Diameter	3" [7.6 cm]
Straps Per Reel	20,000 (Nominal)
Reels per Box	3 Reels

Figure 11 - SOT Pin Configuration and Footprint

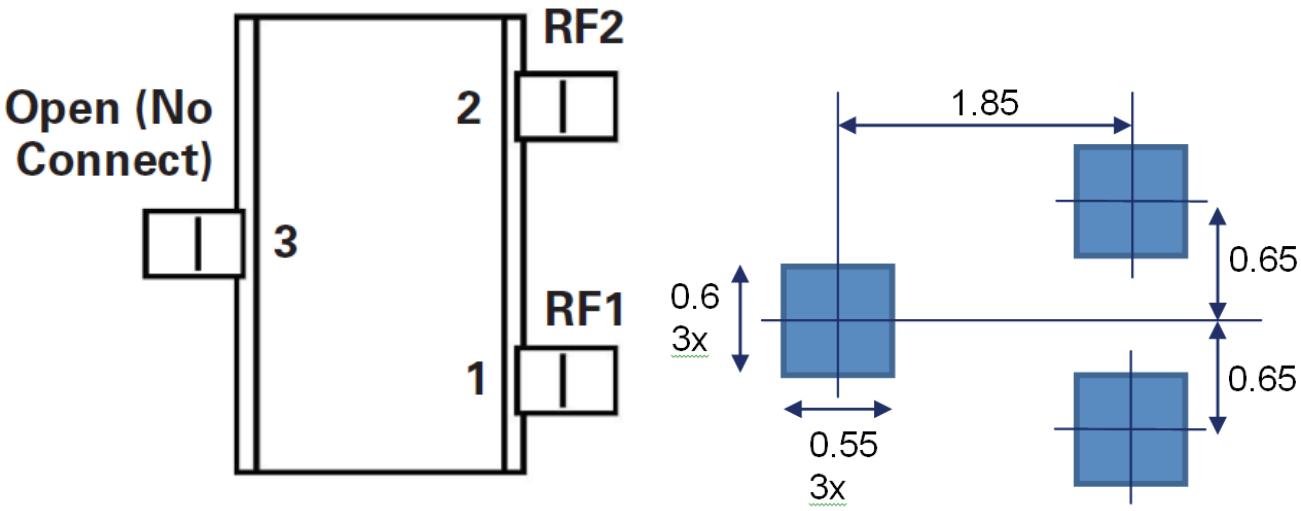
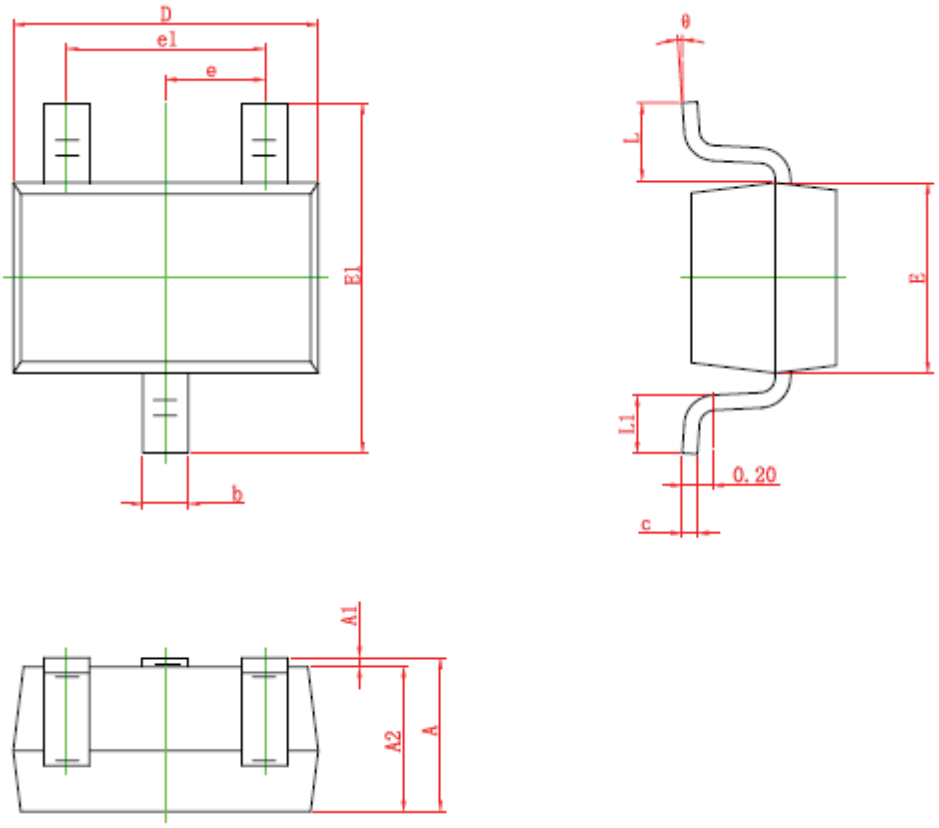


Table 9.2- SOT Pin Description

Pin #	Pin Name	Description
1	RF1	RFID antenna RF connection
2	RF2	RFID antenna RF connection for differential antenna or GND for single ended designs
3	Open	Do not connect

Figure 12 - SOT Dimension Details



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.200	0.400	0.008	0.016
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

Figure 13- SOT Tape Dimensions

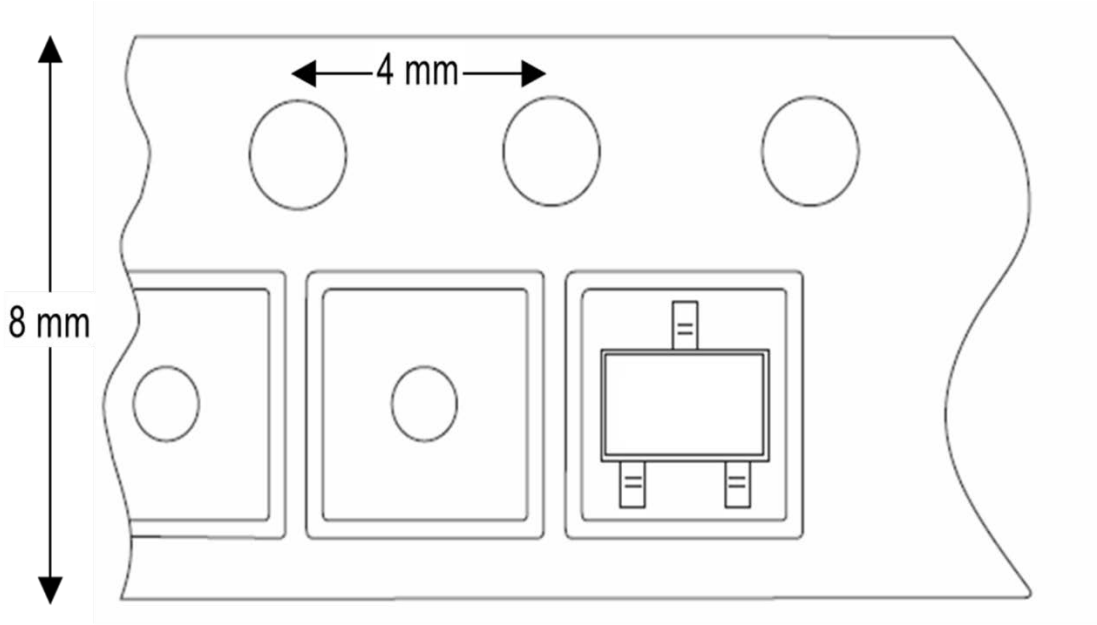
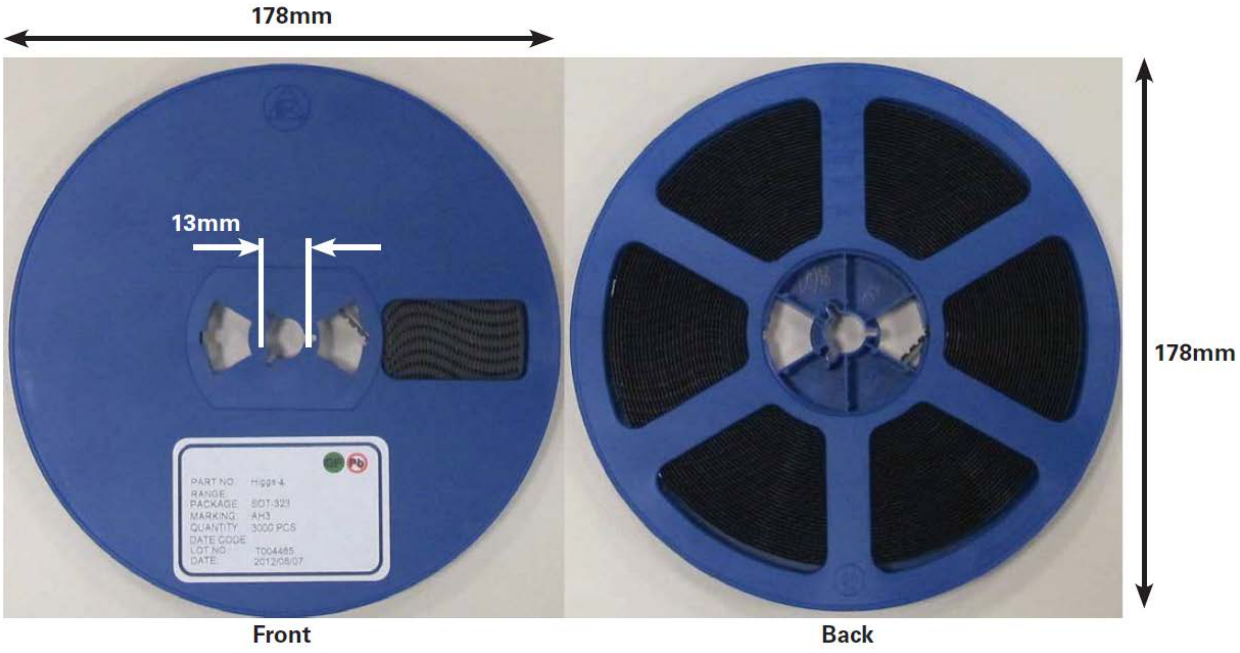


Figure 14 - SOT Reel Dimensions



9.3 Ordering Information

Table 9.3- Ordering Information

Part	Model Number	Description
Higgs™ 4 IC	ALC-370-IC	Bumped, Tested, Ground & Sawn IC's. Provided on 8 Inch Wafer, UV Tape Mounted (SEMI/JIS Standard Metal Film Frame)
	ALC-370-SOT	SMD Package: SOT-323
	ALC-370-FS-CU	Strap, Copper on Kapton: JDEC MO-283

HANDLING PRECAUTIONS Observe standard handling practices to minimize ESD.

DISCLAIMER Application recommendations are guidelines only - actual results may vary and should be confirmed. This is a general purpose product not designed or intended for any specific application.

This product is covered by one or more of the following U.S. patents: 7967204, 7931063, 7868766, 7737825, 7716208, 7716160, 7688206, 7671720, 7659822, 7619531, 7615479, 7598867, 7580378, 7576656, 7562083, 7561221, 7559486, 7559131, 7554451, 7551141, 7542301, 7542008, 7522055, 7500610, 7489248, 7453705, 7452748, 7425467, 7417306, 7411503, 7385284, 7377445, 7364084, 7353598, 7342490, 7324061, 7321159, 7301458, 7295114, 7288432, 7265675, 7262686, 7193504, 7173528, 7172910, 7172789,7141176, 7113250, 7101502, 7080444, 7070851, 7068224, 7046328, 6998644, 6988667, 6985361, 6980184, 6970219, 6952157, 6942155, 6933848. Other patents pending.

October 2016