Kovio 2Kb RFID Tag

Functional Specification

Product Features

1. Passive
2. 13.56MHz
3. 2Kb One-Time-Programmable Memory
4. 7 Bytes Factory Programmed Unique ID
5. 1.8Kb User Memory
6. 106Kb/s Data Transfer Rate
7. Reader-Talk-First Mode
8. CRC and Parity Data Integrity
9. Operating Range of a Few Centimeters

Table of Contents

1. ORDERING INFORMATION

Contact Kovio for ordering options.

2. OVERVIEW

The Kovio 2Kb RFID adheres to the ISO14443 Type A RFID communications standard. It contains a 2,048-bit One-Time-Programmable (OTP) memory block which provides the ability to store up to 1,888 bits of user data. The memory is organized logically as 32-bit (4-byte) pages.

Table 1. K14T3N IC Chip Operating Conditions

Internal Vcc	1.8V (Typical)
Forward Voltage Drop	0.55V (Typical)
Total Capacitance	17pF (Typical)
Frequency	13.56MHz
Communication Standard	ISO14443A Capable of being formatted to support NFC Forum Type 2 Tag
Memory	2Kb one-time-programmable non-volatile memory
Data Transfer Rate	106 Kb/s
Data Integrity	16 bit CRC and Parity bit
Anti-collision	ISO 14443-3 Type A. Supports NFC Forum Type 2 Cascade Level 2

3. BLOCK DIAGRAM

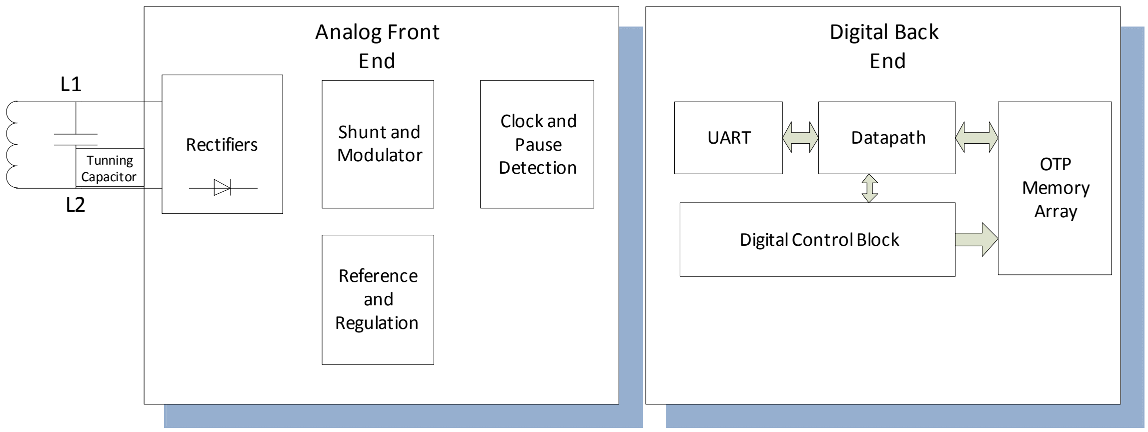


Figure 1. Block Diagram

4. IC LAYOUT

- Chip size: 0.72 X 0.71 mm^2 (w/o scribe line)
- Scribe line width: 80um
- Thickness: 120 µm ± 15 µm
- Pad size: 67 X 67 um^2
- Pad coordinates:
  - Pad L1: X=63.5um, Y=646.5um
  - Pad L2: X=656.5um, Y=63.5um

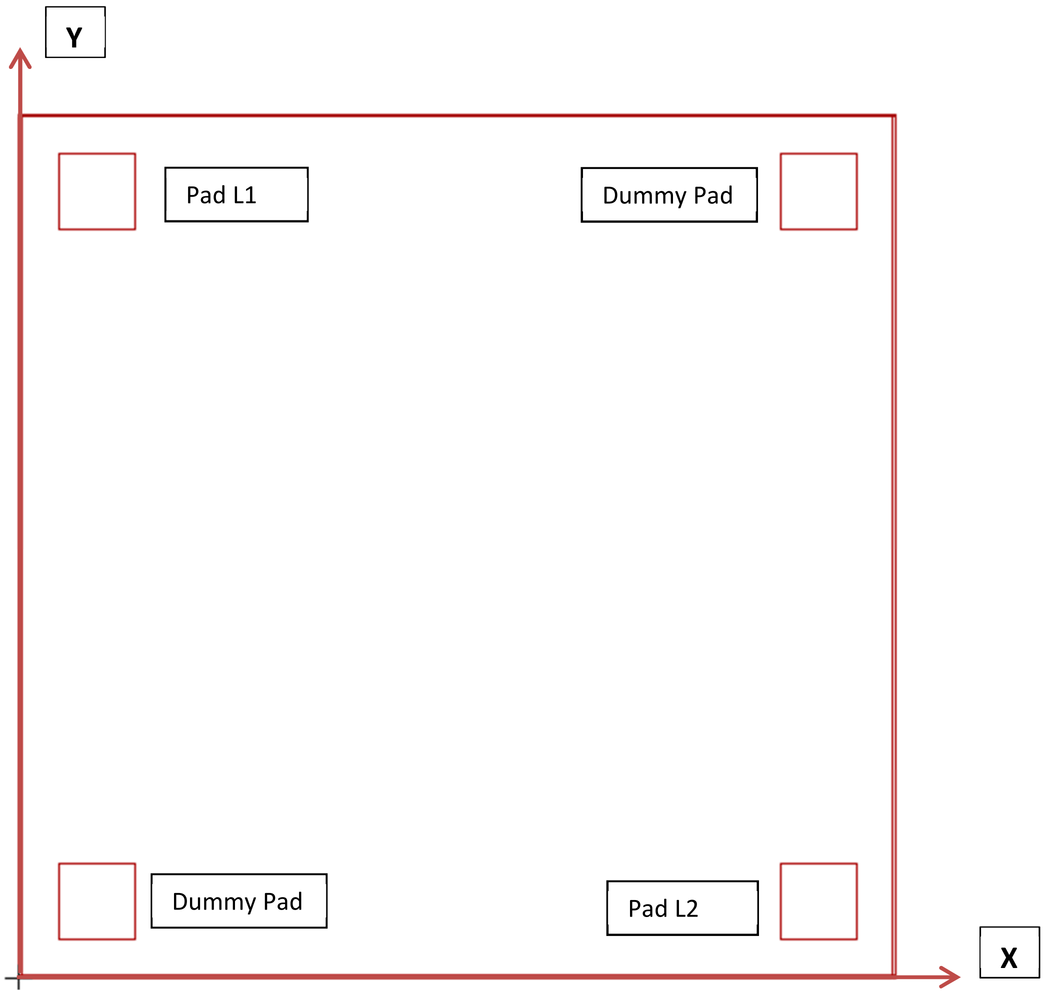


Figure 2. IC Layout

5. OPERATIONAL CHARACTERISTICS

The basic air interface communications protocol is defined in ISO14443 parts 2 and 3. It also adheres to NFC Forum Digital Protocol specifications.

The memory functionality is implemented with a 2,048-bit One-Time-Programmable (OTP) memory to store and retrieve information, of which 1,888 data bits are available to the user as data storage and 56 bits are allocated to the IC's unique identification code. A blank tag is capable of being formatted to be compatible with the NFC Forum Type 2 Tag standard: the 32 bits of memory Page 3 can be allocated to the Capability Container defined in the NFC Forum Type 2 Tag Operation Specification.

6. PHYSICAL LAYER

The basic air interface communications protocol conforms to the ISO14443 Type A air interface specifications as outlined below.

6.1 Air Interface

The communications interface is fully compliant with ISO14443-2, Type A (section 8). Reader-to-tag communications use a 106 Kb/s data rate, employing Modified Miller encoding and 100% ASK modulation. Tag-to-reader communications also use a 106 Kb/s data rate, with 10% OOK load modulated subcarrier at 847 kHz (13.56 MHz / 16) with Manchester bit encoding for the data. All frame communication formats follow ISO14443 Part 2 and 3, Type A. The resonant frequency of the IC is tuned to 15.0MHz with a 17pF on-chip capacitor in the IC.

Table 2. Modulation Characteristics

Modulation	ASK
Data Encoding	Manchester Encoding
Duty Cycle	50% (Typical)
Manchester Subcarrier Period	1.18 us (Typical)
Manchester Subcarrier Frequency	847.5 KHz (Typical)

7. TAG INITIALIZATION AND OPERATION

7.1 State Diagram and States Description

Initialization and anti-collision protocols are compliant with ISO14443-3, Type A. The tag will respond to the standard REQA request command and supports selection to Cascade Levels 1 and 2. Figure 3 shows the state diagram.

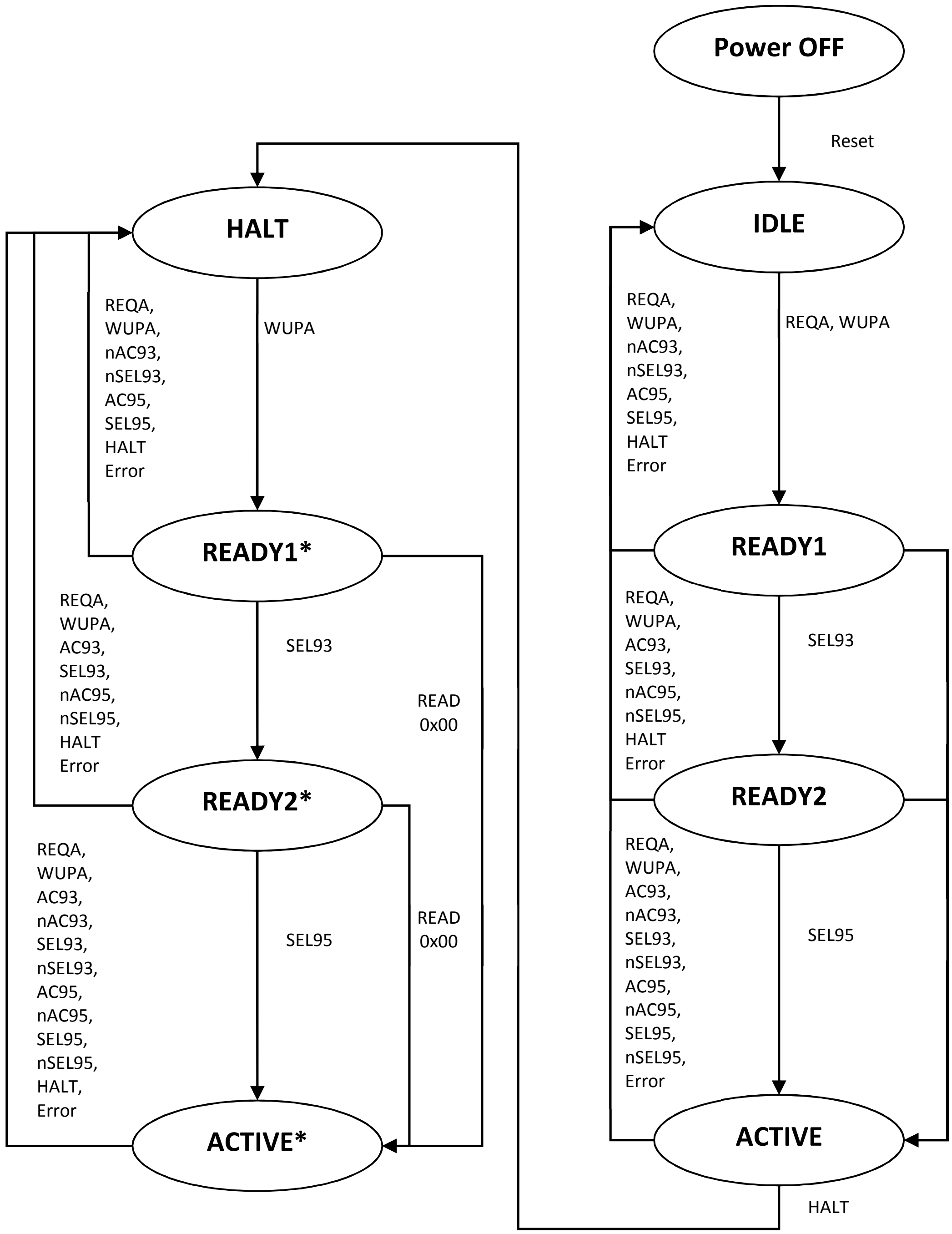


Figure 3. State Diagram

7.1.1 IDLE State

The tag is powered-up into the IDLE state. In this state, it shall listen and recognize REQA and WUPA commands. The tag enters the READY state after it has responded with its ATQA to a valid REQA or WUPA command.

7.1.2 READY State

In the READY state, the bit frame anti-collision mechanism is applied. Cascade level 2 is handled to get the complete UID. The tag enters the ACTIVE state when it is selected with its complete UID.

7.1.3 ACTIVE State

In the ACTIVE state, a READ or WRITE command can be performed. The tag enters the HALT state when a valid HALT command is received.

7.1.4 HALT State

In the HALT state, the tag responds only to a WUPA command. The HALT state assists the reader in the anti-collision mechanism to distinguish between processed tag and unselected tag. The tag enters the READY* state after it receives a valid WUPA command and responded its ATQA.

7.1.5 READY* State

The READY* state is similar to the READY state that the bit frame anti-collision mechanism can be applied. Cascade level 2 is handled to get the complete UID. The tag enters the ACTIVE* state when it is selected with its complete UID.

7.1.6 ACTIVE* State

The ACTIVE* state is similar to the ACTIVE that a READ or WRITE command can be performed. The tag enters the HALT state when it receives a valid HALT command.

7.2 Frame Formats

All communications between the reader and tag follow the ISO14443-2 Type A specifications; transmissions of commands and data are framed with a Start bit (S) and End-of-communication (E). Two framing types are supported, a short and a standard frame. Example of a short frame, defined in the ISO14443-3, is the REQA command shown in Figure 4 where S is the Start-of-transmission bit, and E is the End-of-communication marker. Manchester bit coding is used for Tag-to-reader transmissions, while Modified Miller bit coding is used for reader-to-Tag transmissions per ISO14443-2 specification.

Per ISO14443-2, for reader-to-Tag transmissions, the start bit S is a zero bit, and the End-of-communication marker E is a zero bit followed by no modulation for one bit period. For Tag-to-reader transmissions, the start bit S is a 1 bit, and the End-of-communication marker E is no modulation for a period of one bit.

	LSB						MSB	
S	b1	b2	b3	b4	b5	b6	b7	E

Figure 4. Short Frame

Commands and responses transmitted using the standard frame defined in the ISO14443-3 specification is shown in Figure 5. P is an odd parity bit.

	LSB							MSB								
S	b1	b2	b3	b4	B5	b6	b7	b8	P	b1	b2	…	b7	b8	P	E
Start bit	1st byte								1st Parity bit	2nd byte			Nth byte		Nth Parity bit	End comm

Figure 5. Standard Frame

The time delay from the end of a command transmission by a reader until the start of reply modulation by the Tag is defined as the frame delay time (FDT) and is determined according to ISO14443-3.

7.3 Command Set

The following commands used by the reader to manage communication with the Tags.

7.3.1 REQA Command

Table 3. REQA Command

Command/Response	Code	Description
REQA	0x26 (7 bits)	Upon receiving this command in the IDLE state, the Tag responds with its ATQA and enters the READY1 state. The Tag only responds to this command when in the IDLE state and if the command is received when the tag is in any other state, the Tag returns to the waiting state (IDLE or HALT).
ATQA	0x0044	The Tag responds to both REQA or WUPA command with the ATQA response. The value 0x0044 indicates double size UID (7 bytes) and support for bit level anti-collision.

REQA and ATQA are implemented fully according to ISO14443-3, Type A.

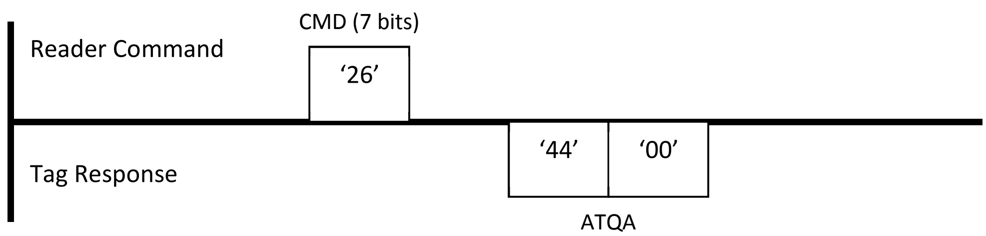


Figure 6. REQA Command

7.3.2 WUPA Command

Table 4. WUPA Command

Command/Response	Code	Description
WUPA	0x52 (7 bits)	Upon receiving this command in the IDLE or HALT state, the Tag responds with its ATQA and enters the READY1 state. The Tag does not respond in any other states.
ATQA	0x0044	The Tag responds to both REQA or WUPA command with the ATQA response. The value 0x0044 indicates double size UID (7 bytes) and support for bit level anti-collision.

WUPA is implemented fully according to ISO14443-3, Type A.

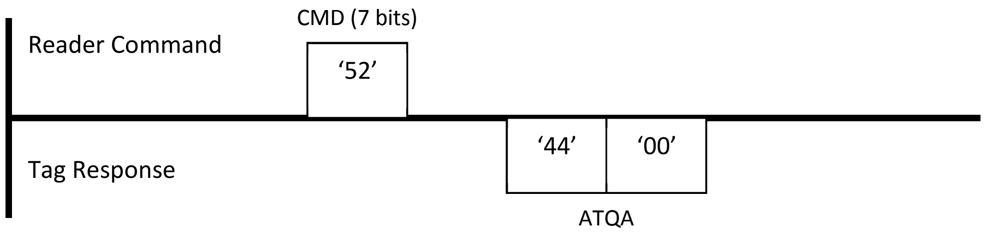


Figure 7. WUPA Command

7.3.3 Anti-Collision and Select of Cascade Level 1

Table 5. Anti-Collision and Select of Cascade Level 1

Command/Response	Code	Description
AC93	0x93, 0x20-0x67, Part of UID CL1	Upon receiving this command in the READY1 state, the Tag remains at its current state and responds with part of UID for Cascade Level 1. The Tag does not respond in any other states and returns to the waiting state (IDLE or HALT).
Part of UID CL1	0x88, part of UID CL1	The Tag responds with remainder of the Cascade Level 1 UID.

It is compliant to ISO14443-3, Type A anti-collision loop.

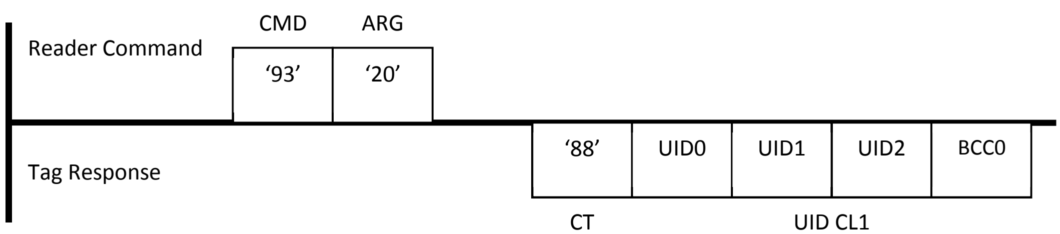


Figure 8. Anti-Collision of Cascade Level 1

Table 6. Select of Cascade Level 1

Command/Response	Code	Description
SEL93	0x93, 0x70, 0x88, UID0, UID1, UID2, BCC0, CRCA	Upon receiving this command in the READY1 state, the Tag responds with SAK1 and enters to the READY2 state.
SAK1	0x04, CRCA	Select Acknowledge for Cascade Level 1 and Cascade bit is set for UID not complete.

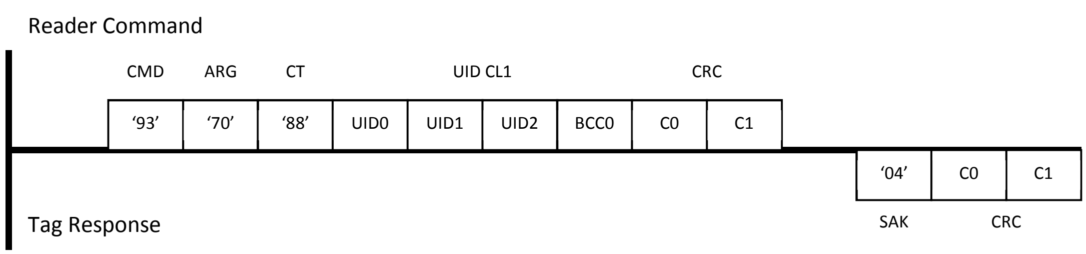


Figure 9. Select of Cascade Level 1

7.3.4 Anti-Collision and Select of Cascade Level 2

Table 7. Anti-Collision and Select of Cascade Level 2

Command/Response	Code	Description
AC95	0x95, 0x20-0x67, part of UID CL2	Upon receiving this command in the READY2 state, the Tag remains at its current state and responds with part of UID for Cascade Level 2. The Tag does not respond in any other states and returns to the waiting state (IDLE or HALT).
Remaining part of UID CL2	Remaining part of UID CL2	The Tag responds with the remaining part of UID CL2.

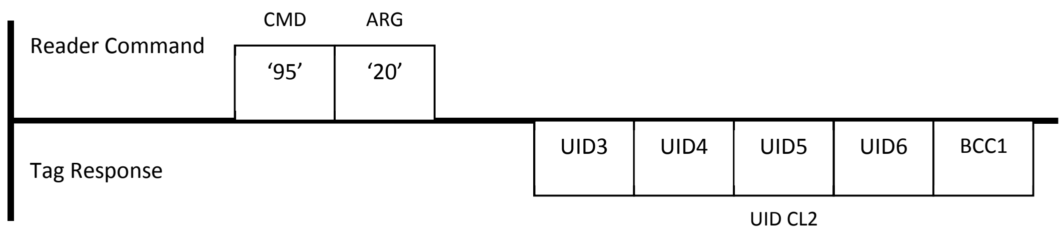


Figure 10. Anti-Collision of Cascade Level 2

Table 8. Select of Cascade Level 2

Command/Response	Code	Description
SEL95	0x95, 0x70, UID3, UID4, UID5, UID6, BCC1, CRCA	Upon receiving this command in the READY2 state, the Tag responds with SAK2 and enters to the ACTIVE state.
SAK2	0x00, CRCA	Select Acknowledge for Cascade Level 2 and complete anti-collision loop.

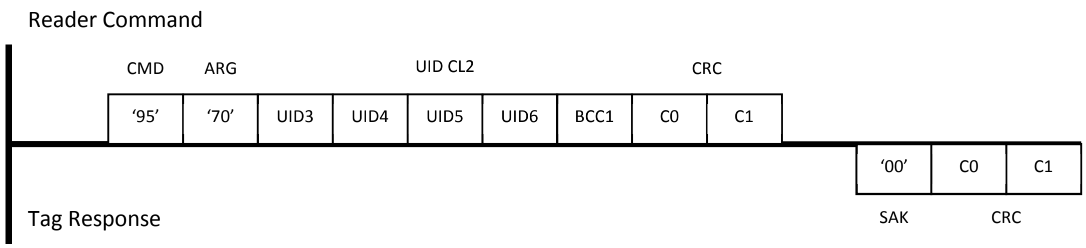


Figure 11. Select of Cascade Level 2

7.3.5 HALT Command

Table 9. HALT Command

Command/Response	Code	Description
HALT	0x50, 0x00, CRCA	This command is set the processed Tags into HALT state instead of IDLE state.
Passive ACK or NACK	No response or 0x5 (4 bits)	Passive ACK with no response. Or The Tag responds with unsuccessful command.

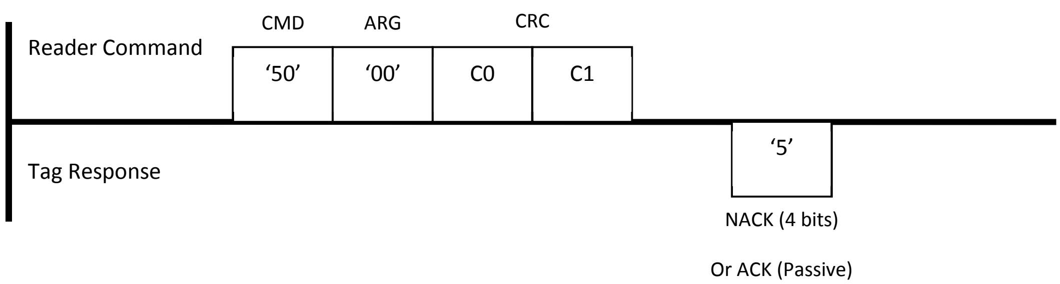


Figure 12. HALT Command

7.3.6 READ Command

Table 10. READ Command

Command/Response	Code	Description
READ	0x30, ADDR, CRCA	This command is to transmit 16 bytes starting from the page address defined in the command. A loop around of the memory read is also implemented. For example, a read starting from pages address 63 will read pages 63, 0, 1 & 2 in that order.
16 bytes data or NACK	16 bytes data, CRCA or 0x1 (4 bits)	The Tag responds with 16 bytes of data starting from the page number defined in the READ command. Or The Tag responds with unsuccessful READ command.

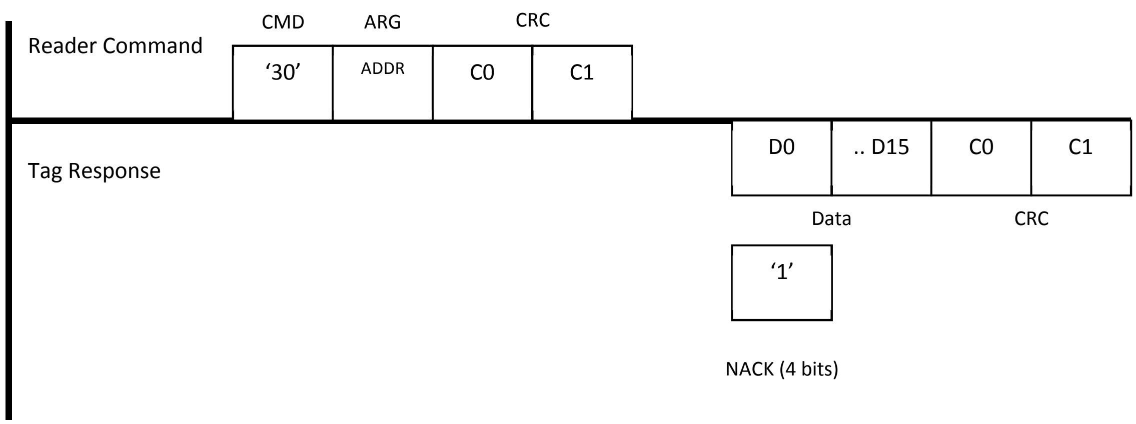


Figure 13. READ Command

7.3.7 WRITE Command

Table 11. WRITE Command

Command/Response	Code	Description
WRITE	0xA2, ADDR, 4 byte data, CRCA	This command is to program one page (4 bytes of data). The page can be the capability container page, lock bytes or data area. If a bit is already programmed to "1," then it cannot be changed back to a "0." The WRITE command and current contents are bit-wise "or-ed" and the result is the new content.
ACK or NACK	0xA (4 bits) or 0x1 (4 bits)	The Tag responds with a successful or unsuccessful completion.

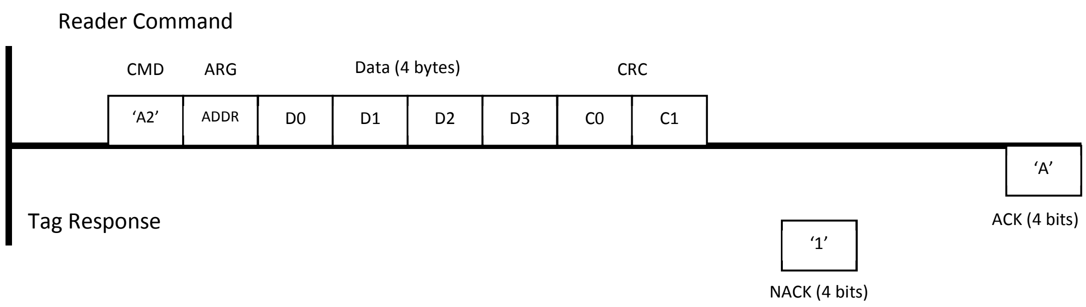


Figure 14. WRITE Command

7.3.8 Coding of ATQA

MSB															LSB
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
RFU				Proprietary				UID size		RFU	Bit frame anti-collision				

Figure 15. Coding of ATQA

- All RFU bits shall be set to 0.
- UID size is set to 01b indicating double UID (7 bytes)
- Bit frame anti-collision is set with 00100b

The coding of ATQA for the Tag is 0x0044 indicating RFU and proprietary bits are set to “0,” UID size is double (7 bytes) and bit-oriented anti-collision is supported.

8. MEMORY STRUCTURE

8.1 Memory Organization

The Tag contains 2,048 bits of OTP memory, organized into 64 4-byte pages.

The initial state of the memory is read as logical "0." A programmed state is read as logical "1." Once any bit is programmed to "1," it cannot be erased.

The memory organization contains:

- UID & BCC: Unique identifier and its check bytes
- Internal: Reserved for manufacturing use
- Lock: Switch content from Read/Write to Read-Only
- Data: User data to store information
- Counter: One or more data pages can be used as incremental counter if application requires.

	Memory Organization			
Page	**Byte0**	**Byte1**	**Byte2**	**Byte3**
0	UID0	UID1	UID2	BCC0
1	UID3	UID4	UID5	UID6
2	BCC1	Internal	Lock0	Lock1
3	CC0	CC1	CC2	CC3
4	Data0	Data1	Data2	Data3
5	Data4	Data5	Data6	Data7
6	Data8	Data9	Data10	Data11
7	Data12	Data13	Data14	Data15
. . .				
58	Data216	Data217	Data218	Data219
59	Data220	Data221	Data222	Data223
60	Data224	Data225	Data226	Data227
61	Data228	Data229	Data230	Dat231
62	Lock2	Lock3	Lock4	Lock5
63	Lock6	Lock7	Reserved	Reserved

Figure 16. Memory Organization

8.2 Unique Identifier

Page 0, Page 1, and the first byte of page 2 of the memory contain the 7 byte UID and its two check bytes. After programming the UID, the 7 UID bytes and the two check bytes are automatically write-protected.

Check byte0 (BCC0) = CT (XOR) UID0 (XOR) UID1 (XOR) UID2
Check byte1 (BCC1) = UID3 (XOR) UID4 (XOR) UID5 (XOR) UID6

CT is defined as 0x88.

UID0 shall contain the Integrated Circuit Manufacturer ID number for Kovio, 0x37, per ISO/IEC 14443-3 and ISO/IEC 7816-6/AM1.

8.3 Internal

The internal bytes are reserved for manufacturing use. The Tag shall not use the internal bytes to store information data.

8.4 LOCK Bytes

In order to prevent the data that has been written in the data area from being overwritten, the Tag provides the lock bytes feature. Once the lock byte has been programmed, the corresponding memory content switches from Read/Write to Read-Only. Lock bytes can lock several pages at a time, or individual bits within the lock byte can be programmed to lock individual pages. There are also five block-locking bits to freeze the locking configuration. Using the lock bytes feature does not affect the reading of the tags.

There are in total eight programmable lock bytes. Referring to Figure 16, the lock bytes are located in: Page 2 (Bytes2 and Bytes 3), Page 62 (Byte0, Byte1, Byte2 and Byte3) and Page 63 (Byte0 and Byte1). Following this same order, the Lock bytes are then numbered Lock0 (Page 2, Byte2) to Lock 7 (Page 63, Byte1).

Figure 17 shows the organization of the eight programmable lock bytes. For page locking, the number following the “L” denotes which page is controlled by that bit. For example, bit 4 of locking byte Lock0 will lock page 4 in the memory area. So if this bit is programmed to a “1”, whatever is currently written into page 4 in the memory area cannot be changed. No additional WRITE command can be performed on page 4.

The five block-locking bits are found at the following locations:

- Lock0, bit 0 (controls the locking configuration for page 3)
- Lock0, bit 1 (controls the locking configuration for pages 4-9)
- Lock0, bit 2 (controls the locking configuration for pages 10-15)
- Lock7, bit 6 (controls the locking configuration for pages 16-47 and the locking of page 62)
- Lock7, bit 7 (controls the locking configuration for pages 48-63 and the locking of page 63)

If a block-locking bit is locked (programmed to a “1”), then the lock bytes to those corresponding pages cannot be changed. For instance, if Lock0, bit 1 is programmed to “1”, then the lock bytes (and hence the locking configuration) for pages 4-9 cannot be changed.

Lock bytes can be programmed with WRITE command. BCC1 and Internal byte shall not be affected by corresponding WRITE command.

The Tag lock status is updated immediately after the WRITE command is executed.

	MSB (bit 7)							LSB (bit 0)
Lock0	L7	L6	L5	L4	L3	BL 10-15	BL 4-9	BL 3
Lock1	L15	L14	L13	L12	L11	L10	L9	L8
…								
Lock6	L55	L54	L53	L52	L51	L50	L49	L48
Lock7	L63 BL 48-63	L62 BL 16-47	L61	L60	L59	L58	L57	L56

Figure 17. Lock Bytes Configuration

If an attempted WRITE command is performed on a locked page, the Tag shall not perform the WRITE operation and shall respond with a NACK, except for page 2.

8.5 Data

Pages 3 to 61 represent the data pages for the user to store information.
All bytes in the data area are initially blank: 00h.

8.6 Counter

One or more data pages can be used as incremental counter (programming one bit at a time) if required by the application. For a one-page counter, use of page 61 is recommended. Bits can be programmed from “0” to “1” but cannot be erased from “1” to “0”.

8.7 Formatting as an NFC Forum Type 2 Tag

This RFID tag is capable of being formatted to comply with the NFC Forum Type 2 Tag standard. To format the tag, program the following data to pages 3 and 4.

The Capability Container, stored in the 4 bytes of page 3, (CC) contains NFC Forum management data:

Page 3, Byte 0 is E1h, indicating the NFC Forum "magic number"
Page 3, Byte 1 is 10h, indicating the version number of the mapping NFC document: version 1.0
Page 3, Byte 2 is 1Dh, indicating the memory size of the data area: 232 bytes
Page 3, Byte 3 is 00h, indicating that read and write operations are permitted

Page 4, Byte 0 is 03h, indicating formatting for an NDEF message.

9. INLAY

9.1 Example Inlay Components / Form Factor

Table 12: Inlay Components/Form Factor for ID1 (Credit card / ticket size) Inlay

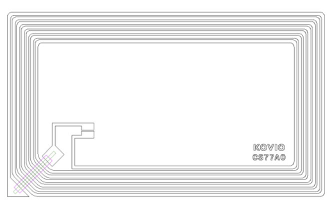
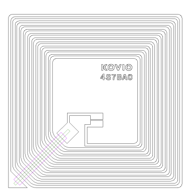
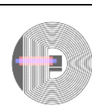
Antenna width	76.0mm ±1mm*
Antenna height	44.0mm ±1mm*
Height without IC	0.07mm
Height with IC	0.21mm

Parameters shall be within 5% tolerance unless otherwise noted.

Shown below is a typical example of an antenna, with 500 µm line width, and 500 µm spacing, a 2 mil PET substrate and a conductive strap on top of an insulation layer. Other designs can be used for specific customer requirements.

9.2 Physical Layout

Table 13. Physical Layout of Antennas

Size	**Antenna Shape**
76 x 44mm	
42 x 42mm	
24mm diameter Circular	

10. ELECTRICAL CHARACTERISTICS AND RELIABILITY

Table 14. Electrical and Reliability

Parameters	Values
Frequency	13.56MHz
Data Retention	5 years
Bending Diameter	>30mm

10.1 Characteristics

Table 15. Characteristics

Parameter	Minimum	Typical	Maximum	Units
Peak Repetitive Reverse Voltage			2.5	V
RMS Reverse Voltage			1.8	V
Peak Forward Current			30	mA
Power Dissipation			50	mW
Reverse Breakdown Voltage			3.6	V
Operating Temperature	-20		+60	°C
Storage Temperature	-20		+60	°C
ESD (Human Body Model)			2,000	V

11. TABLES

12. FIGURES

13. REVISION HISTORY

Section	Description
Revision 2.0 (March 2, 2012)	
	Comprehensive update